Claims

1. Circuit for clock synchronization between a first and second network unit (NTDM, NP), with a clock recovery unit (CR) for provision of at least one reference clock signal (RCLKn) being provided in the first network unit (NTDM), characterized in that
at least one bus provision unit (CHn) with at least one encoding unit (KKn) is arranged in the first network unit and one encoding unit (KKn) in each case is used for forming a channel signal (KSn) from the reference clock signal present in each case, with a bus signal (PWDC) being formed from at least one channel signal and forwarded to a decoder unit (DE) in the second network unit (NP).

2. Circuit arrangement in accordance with claim 1, characterized in that
the encoding unit (KKn) is embodied such that a sequence of individual pulses with a defined distance is created from the reference clock signal (RCLKn) present on the input side.

3. Circuit in accordance with one of the previous claims, characterized in that
the encoding unit (KKn) is embodied such that the defined distances of the pulses are characterized differently in each channel signal (KSn).

4. Circuit in accordance with one of the previous claims, characterized in that
the encoding unit (KKn) is embodied such that the number of pulses created in each channel signal (KSn) corresponds to the maximum possible number(s) of the encoding units.

5. Circuit in accordance with one of the previous claims, characterized in that

the encoding unit (KKn) is embodied such that
the width of the pulses created (PW1, PW2,...,PWn) is embodied differently.

6. Circuit in accordance with one of the previous claims, characterized in that
the encoding unit (KKn) is embodied such that
the width of the pulses created (PW1, PW2,...,PWn) is embodied in ascending order.

7. Circuit in accordance with one of the previous claims, characterized in that
the encoding units (KK) are embodied such that,
no distinction is made with regard to pulse width formation below the encoding units.

8. Circuit in accordance with claim 1, characterized in that
the bus provision unit (CHn) is embodied such that the channel signals (KSn) are grouped together via a summation unit (SB) and signal amplification units (BT) into a bus signal (PWDC).

9. Circuit in accordance with claim 1, characterized in that
the second network unit is embodied such that the selection of the individual channel signals from the bus signal (PWDC) is executed independently by the second network unit (NP).

10. Circuit in accordance with claim 1, characterized in that
the decoding unit (DE) features at least one pulse width filter (PWF).

11. Circuit in accordance with one of the previous claims, characterized in that
the decoding unit (DE) features at least one pulse distance

filter (PDF).

12. Circuit in accordance with one of the previous claims, characterized in that
the decoding unit is embodied such that decoding is executed by means of a mask function, in that the received bus signal is not sampled and the selection occurs by masking out the pulses not required.

13. Method for clock synchronization between a first and second network unit (NTDM, NP), with a clock recovery unit (CR) for provision of at least one reference clock signal (RCLKn) being provided in the first network unit (NTDM), characterized in that
a channel signal is formed from a reference clock signal in each case, with, in the first network unit (NTDM) a bus signal (PWDC) being formed from at least one channel signal and forwarded to the second network unit (NP).

14. Method in accordance with claim 13,
characterized in that
a sequence of individual pulses with a defined distance is created from the reference clock signal (RCLKn) present on the input side.

15. Method in accordance with one of the previous claims, characterized in that,
the defined distances of the pulses are characterized differently in each channel signal (KSn).

16. Method in accordance with one of the previous claims, characterized in that,
the number of pulses generated in each channel signal (KSn) corresponds to the maximum possible number(s) of the encoding units.

17. Method in accordance with one of the previous claims, characterized in that,
the width of the pulses created (PW1, PW2,...,PWn) is embodied differently.

18. Method in accordance with one of the previous claims, characterized in that,
the width of the pulses created (PW1, PW2,...,PWn) is embodied in ascending order.

19. Method in accordance with one of the previous claims, characterized in that,
no distinction is made with regard to pulse width formation below the encoding units.

20. Method in accordance with one of the previous claims, characterized in that,
the channel signals (KSn) are grouped into a bus signal (PWDC).

21. Method in accordance with one of the previous claims, characterized in that,
the selection of the individual channel signals from the bus signal (PWDC) is performed independently by the second network unit (NP).

22. Method in accordance with one of the previous claims, characterized in that,
decoding is undertaken in the second network unit (NP) by means of a mask function, in that the received bus signal is not sampled and the selection is made by masking out the pulses not required.